
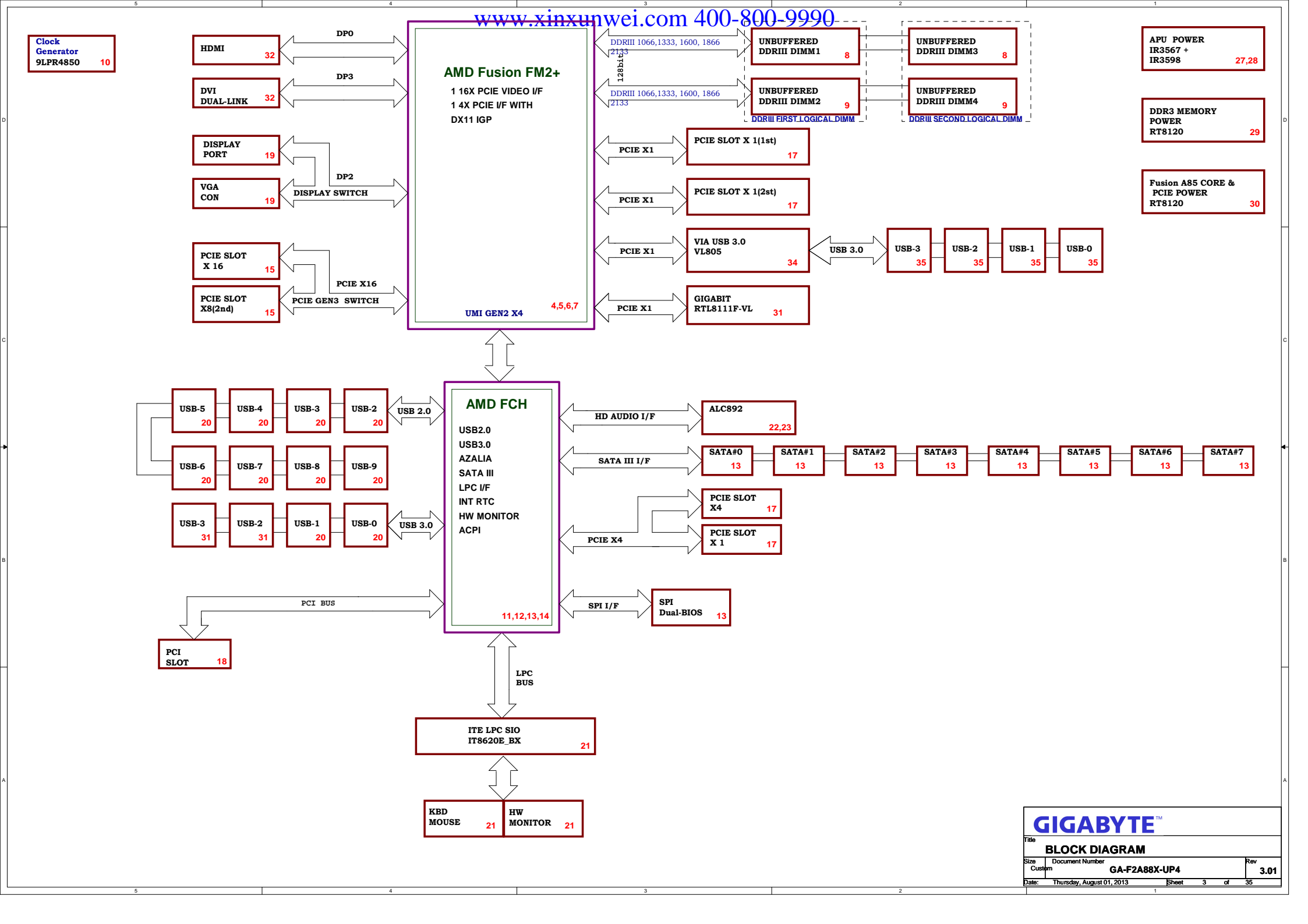


PAGE	TITLE
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GIGABYTE™			
Title COVER SHEET			
Size Custom	Document Number GA-F2A88X-UP4		Rev 3.01
Date:	Monday, August 05, 2013	Sheet	1 of 34

A

				
Title				
BOM & PCB HISTORY				
Size	Document Number			Rev
Custom	GA-F2A88X-UP4			3.01
Date:	Thursday, August 01, 2013	Sheet	2	of 35



FM2 DDR Layout Guide

Ver:1.0

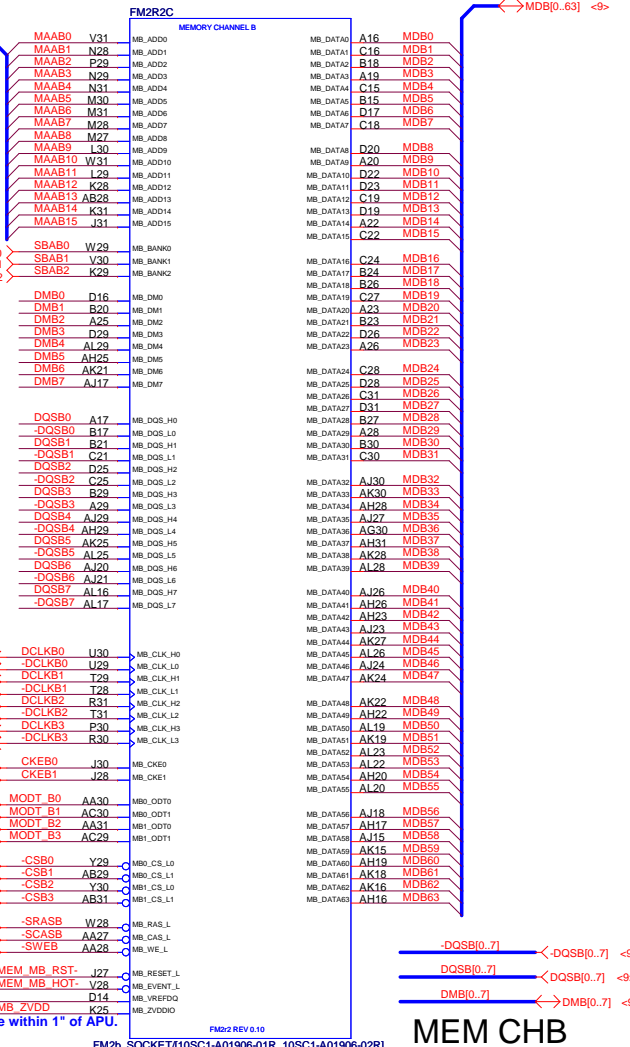
	Impedance	4L-1080-20Z
Clocks	72 ohm	20/7.5/7.5/20
ADDR, CMD, Control	40 ohm	7 mil
DQS	90 ohm	20/5/6/5/20
DATA, DM	40 ohm	7 mil
Others	40-60 ohm	7 mil

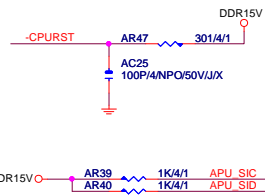
FM2 DDR Layout Guide

Ver:1.01

	Impedance	4L-1080-20Z
Clocks	72 ohm	20/8/5/8/20
ADDR, CMD, Control	40 ohm	8 mil
DQS	90 ohm	20/4.5/7.5/4.5/20
DATA, DM	40 ohm	7 mil
Others	40-60 ohm	4 mil

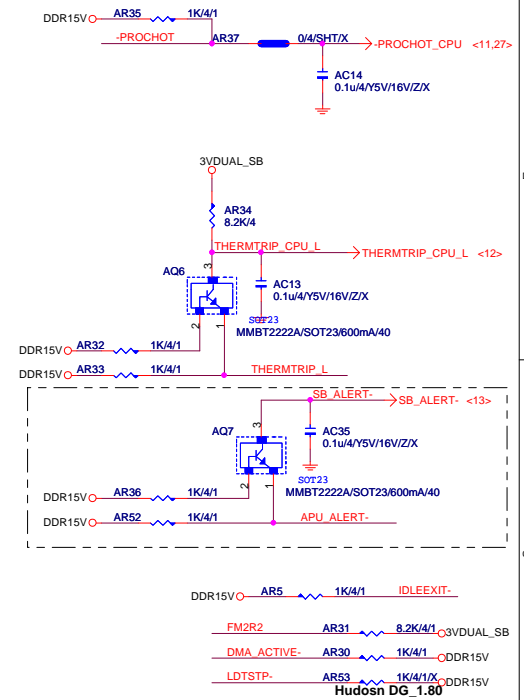
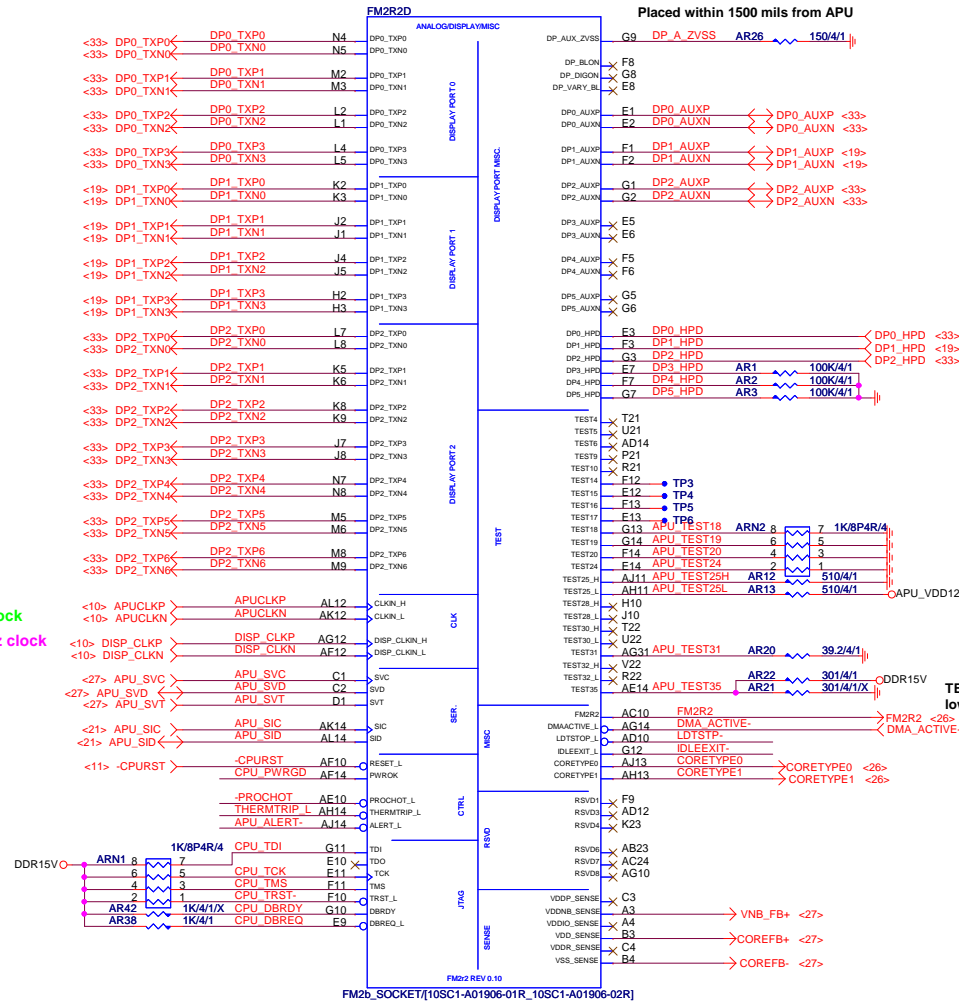
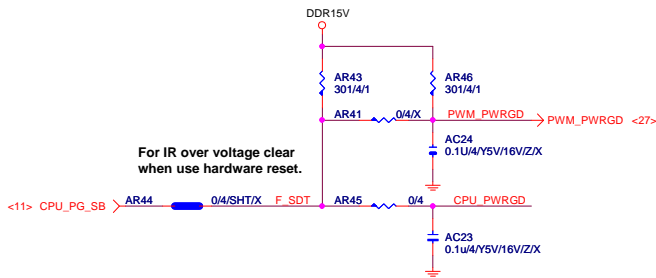
<8> MAA0[0..15]





FM2 CPU Clock Layout Guide

	Impedance	4L-1080
APU Clock	85 ohm	20/4.5/7.5/4.5/20
DISP Clcock	85 ohm	20/4.5/7.5/4.5/20
DP TX/RX	85 ohm	20/4.5/7.5/4.5/20
	55 ohm	4 mil
	40-60 ohm	7 mil



**TEST35: high=>HDMI enable,
low=>HDMI disable.**

	APU FM2
Group A	VDDA25:1.8~2.7V/0.5A
Group A	DDR15V:0.8~2.3V/30A
Group B	VCORE: 0.8~2.0V/120A
Group B	VCORE_NB:1.2V/50A
Group B	VDDP:1.2V/5A
Group B	VDDR:1.2V/5A

Group A must early than Group B

FM2R2A

PCIEXPRESS

EXP A RXP0 AD8
EXP A RXN0 AD9
EXP A RXP1 AC7
EXP A RXN1 AC8
EXP A RXP2 AB5
EXP A RXN2 AB6
EXP A RXP3 AB8
EXP A RXN3 AB9
EXP A RXP4 AA7
EXP A RXN4 AA8
EXP A RXP5 Y5
EXP A RXN5 Y6
EXP A RXP6 Y8
EXP A RXN6 Y9
EXP A RXP7 W7
EXP A RXN7 W8
EXP A RXP8 V5
EXP A RXN8 V6
EXP A RXP9 V8
EXP A RXN9 V9
EXP A RXP10 U7
EXP A RXN10 U8
EXP A RXP11 T5
EXP A RXN11 T6
EXP A RXP12 T8
EXP A RXN12 T9
EXP A RXP13 R7
EXP A RXN13 R8
EXP A RXP14 P5
EXP A RXN14 P6
EXP A RXP15 P8
EXP A RXN15 P9

GRAPHICS

P_GFX_TXP0 AC2
P_GFX_TXN0 AC1
P_GFX_TXP1 AC4
P_GFX_TXN1 AC5
P_GFX_TXP2 AB2
P_GFX_TXN2 AB3
P_GFX_TXP3 AA2
P_GFX_TXN3 AA1
P_GFX_TXP4 AA4
P_GFX_TXN4 AA5
P_GFX_TXP5 Y2
P_GFX_TXN5 Y3
P_GFX_TXP6 W2
P_GFX_TXN6 W1
P_GFX_TXP7 W4
P_GFX_TXN7 W5
P_GFX_TXP8 V2
P_GFX_TXN8 V3
P_GFX_TXP9 U2
P_GFX_TXN9 U1
P_GFX_TXP10 U4
P_GFX_TXN10 U5
P_GFX_TXP11 T2
P_GFX_TXN11 T3
P_GFX_TXP12 R2
P_GFX_TXN12 R1
P_GFX_TXP13 R4
P_GFX_TXN13 R5
P_GFX_TXP14 P2
P_GFX_TXN14 P3
P_GFX_TXP15 N2
P_GFX_TXN15 N1

EXP A RXP[0..15] >> EXP_A_RXP[0..15] <15,16>
EXP A RXN[0..15] >> EXP_A_RXN[0..15] <15,16>
EXP A TXP[0..15] >> EXP_A_TXP[0..15] <15,16>
EXP A TXN[0..15] >> EXP_A_TXN[0..15] <15,16>

TX CAP close to CPU side

P_GPP_TXP0 AF2
P_GPP_TXN0 AF3
P_GPP_TXP1 AE2
P_GPP_TXN1 AE1
P_GPP_TXP2 AE4
P_GPP_TXN2 AE5
P_GPP_TXP3 AD2
P_GPP_TXN3 AD3
P_GPP_TXP4 AC33
P_GPP_TXN4 AC34
P_GPP_TXP5 AC37
P_GPP_TXN5 AC38

0.1u/4X7R/16V/K
0.1u/4X7R/16V/K
0.1u/4X7R/16V/K
0.1u/4X7R/16V/K
0.1u/4X7R/16V/K
0.1u/4X7R/16V/K
0.1u/4X7R/16V/K
0.1u/4X7R/16V/K

A TX0P C AC1
A TX0N C AC2
A TX1P C AC3
A TX1N C AC4
A TX2P C AC5
A TX2N C AC6
A TX3P C AC7
A TX3N C AC8

0.1u/4X7R/16V/K
0.1u/4X7R/16V/K
0.1u/4X7R/16V/K
0.1u/4X7R/16V/K
0.1u/4X7R/16V/K
0.1u/4X7R/16V/K
0.1u/4X7R/16V/K
0.1u/4X7R/16V/K

A TX0P <11>
A TX0N <11>
A TX1P <11>
A TX1N <11>
A TX2P <11>
A TX2N <11>
A TX3P <11>
A TX3N <11>

<32> ML_IP >>
<32> ML_IN >>
<17> PCIE1X1_IP >>
<17> PCIE1X1_IN >>
<17> PCIE1X2_IP >>
<17> PCIE1X2_IN >>
<34> USB3_IP >>
<34> USB3_IN >>

AJ8
AJ7
AH6
AH5
AH9
AH8
AG8
AG7

APU_VDD12 AR25 196/4/1 P_VZDD AJ2

Within 1500mil from APU

FM2b_REV10.10

Within 1500mil from APU

FM2b_SOCKET/[10SC1-A01906-01R_10SC1-A01906-02R]

P_ZVSS

AJ1

P_ZVSS

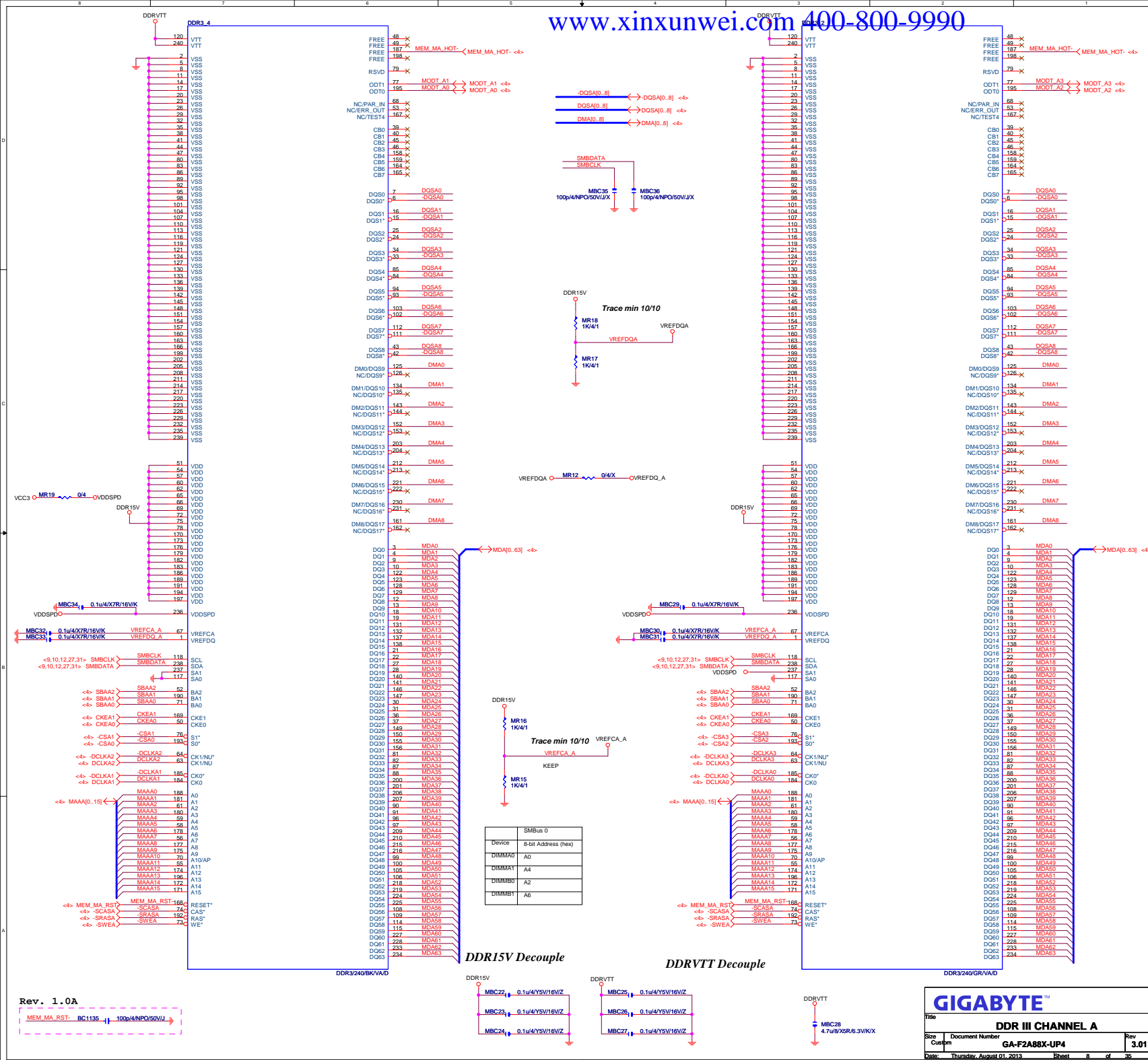
AR24

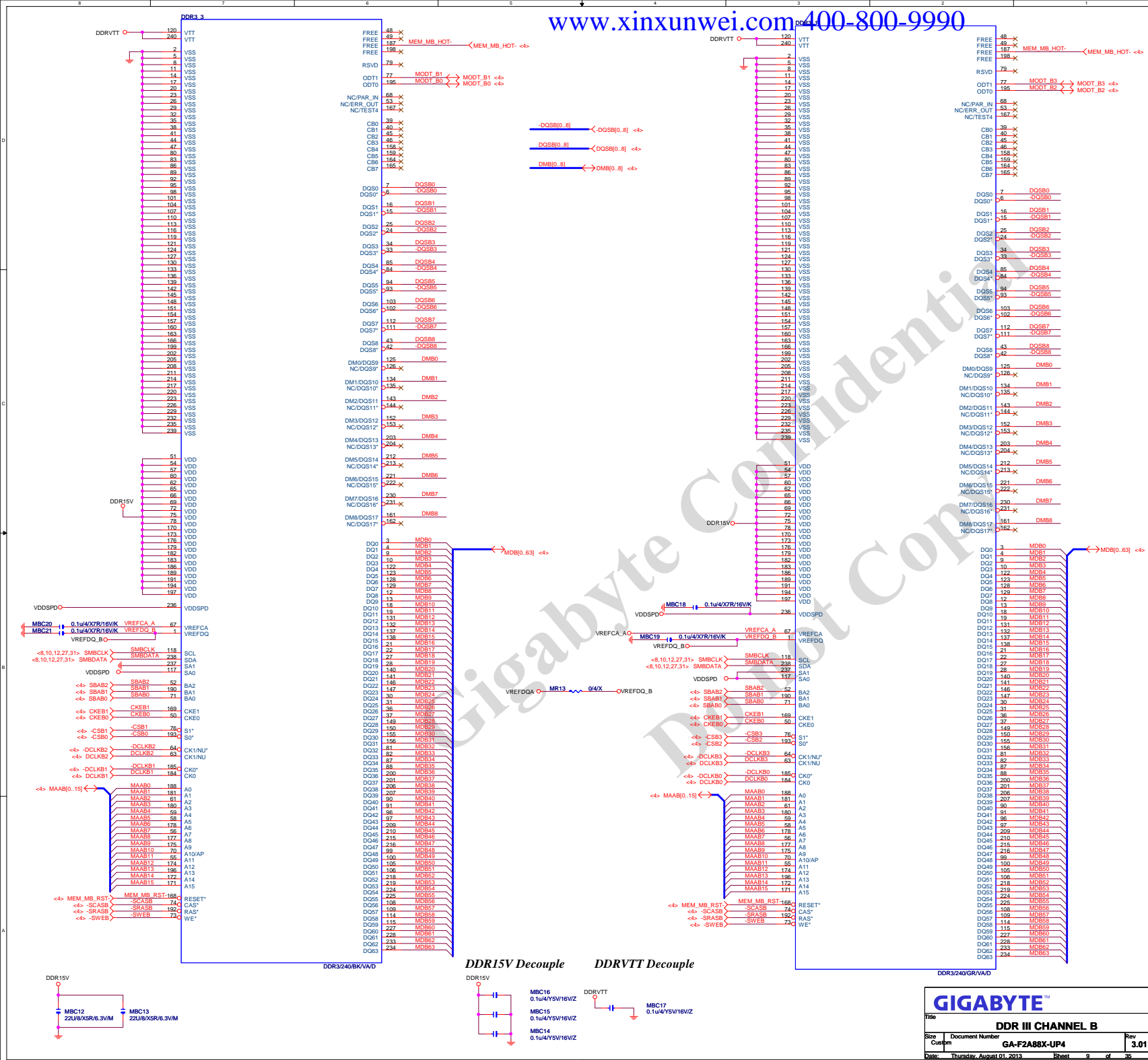
196/4/1

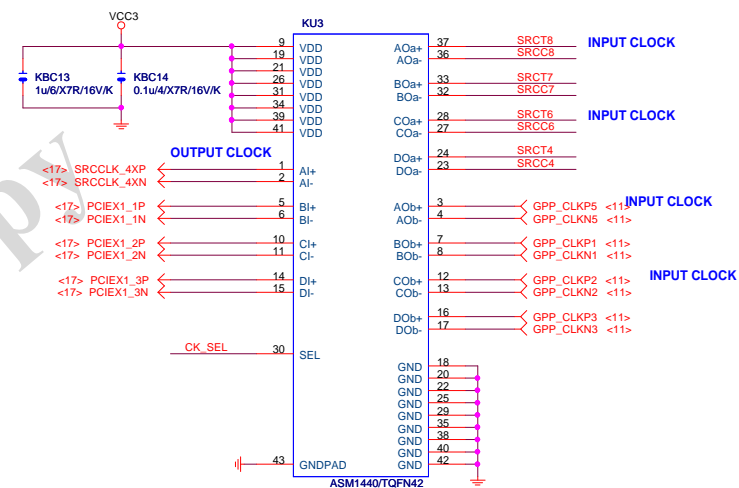
PLACE THESE CAP CLOSE TO APU.

GIGABYTE™

Title			FM2_PCIE LINK		
Size	Document Number	Rev			
Custom	GA-F2A88X-UP4	3.01			
Date:	Thursday, August 01, 2013	Sheet	6	of	35







Function	SEL	CLK source
xl--> xOa	L	External
xl--> xOb	H	Internal

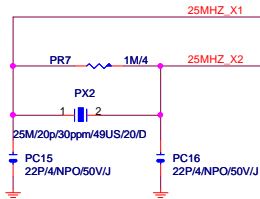
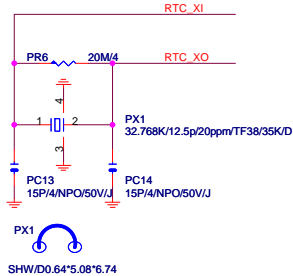
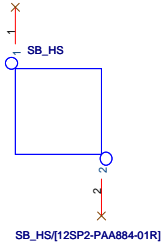
INPUT from Clock Gen

INPUT from South Bridge



PLACE THESE PCIE AC COUPLING CAPS CLOSE TO HUDSON

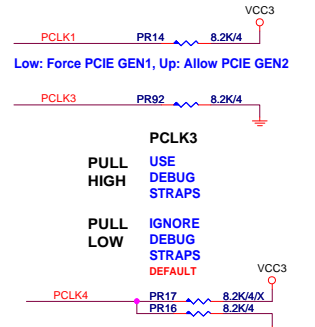
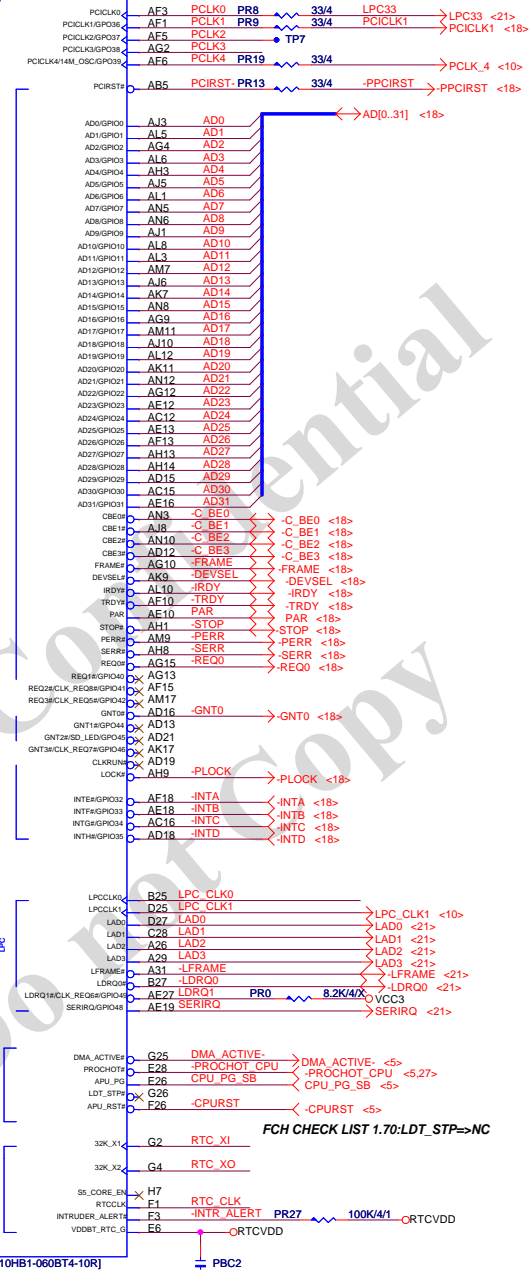
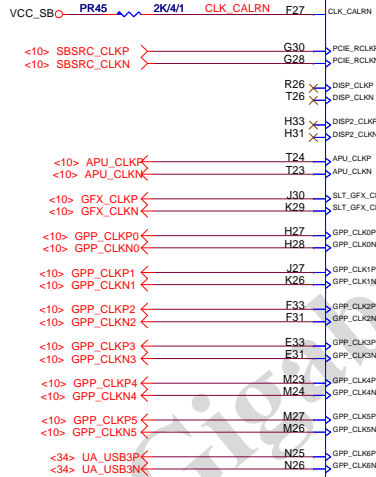
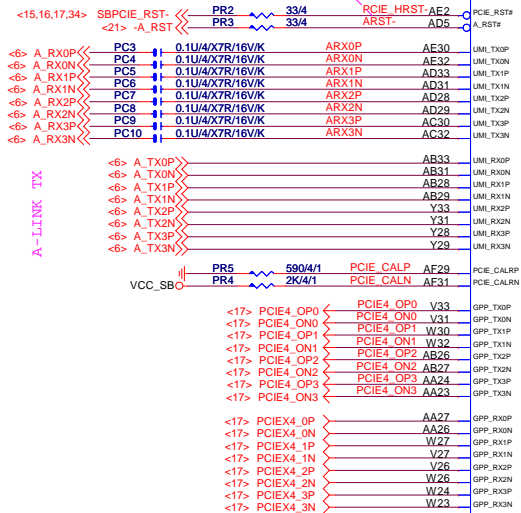
S.B HEATSINK



RTC CLK PR97 8.2K/4
Disable: 10K pull-up to +3.3V_S5.
Enable: 2.2K pull-down.

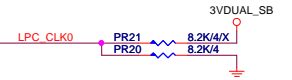
www.xinunwei.com 400-800-9990

PCIE_RST# connect to APU PCIe Devices/Slots

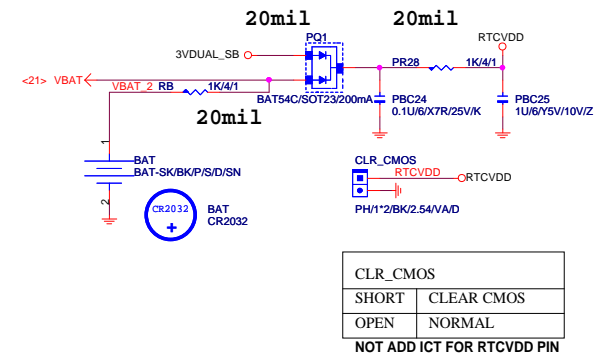


APU_CLKP/N and DISP_CLKP/N Clock Selection
0V Required setting for integrated clock mode.
3.3V Reserved. This strap is not used if the strap CLKGEN is configured for external clock generator mode.

PC1_CLK4
PULL HIGH USE DEBUG STRAPS
PULL LOW IGNORE DEBUG STRAPS DEFAULT



LPC_CLK0 IMC ENABLED AOD Extreme IMC DISABLED DEFAULT
LPC_CLK1 CLKGEN ENABLED CLKGEN DISABLED DEFAULT



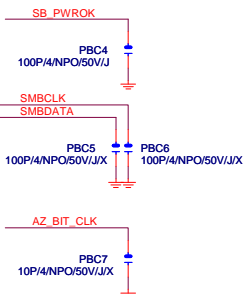
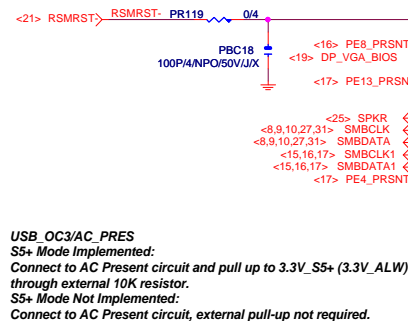
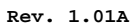
CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL
NOT ADD ICT FOR RTCVDD PIN	

GIGABYTE

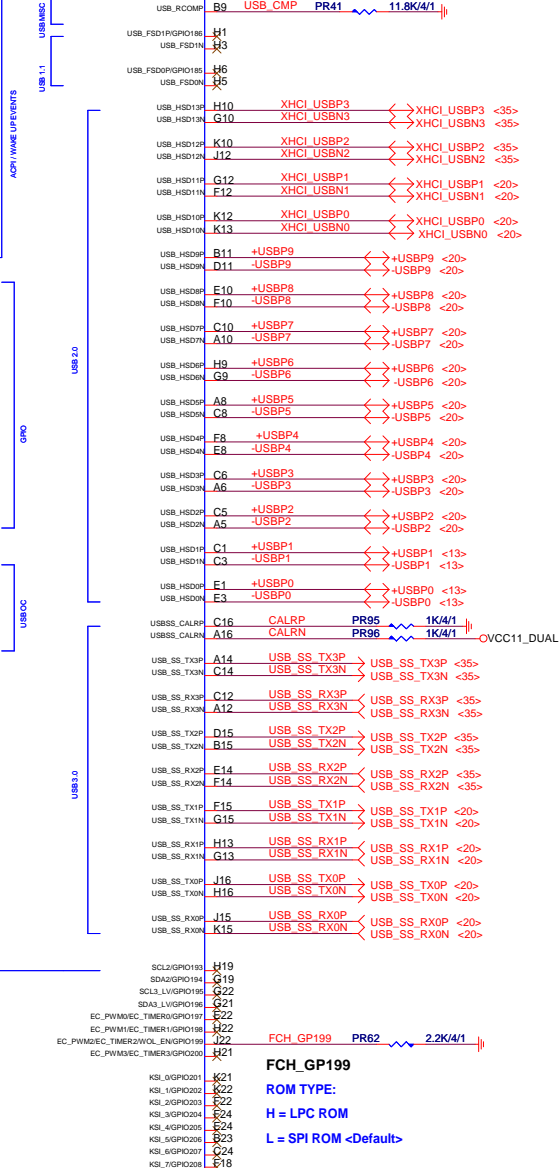
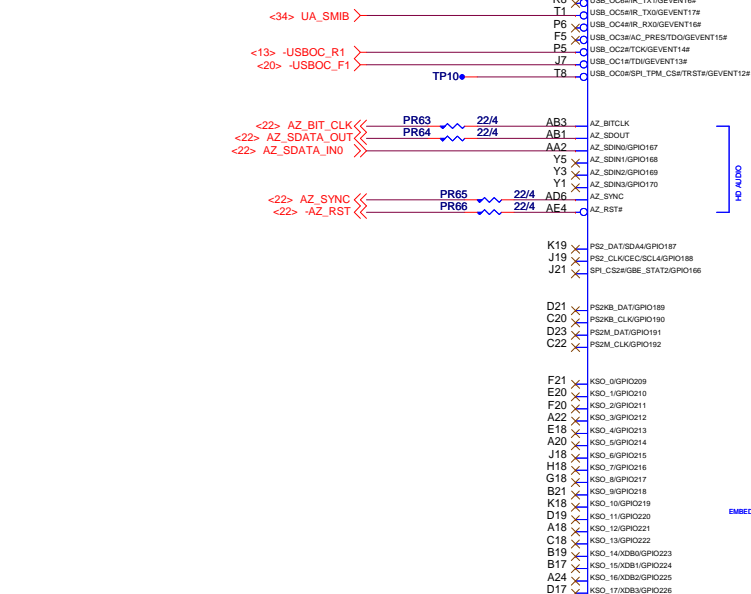
Title: **HUDSON PCIE/PCI/CPU/LPC**

Size: Custom Document Number: **GA-F2A88X-UP4** Rev: **3.01**

Date: Thursday, August 01, 2013 Sheet: 11 of 35



USB_OC3/AC_PRES
S5+ Mode Implemented:
 Connect to AC Present circuit and pull up to 3.3V_S5+ (3.3V_ALW)
 through external 10K resistor.
S5+ Mode Not Implemented:
 Connect to AC Present circuit, external pull-up not required.



FCH_GP199

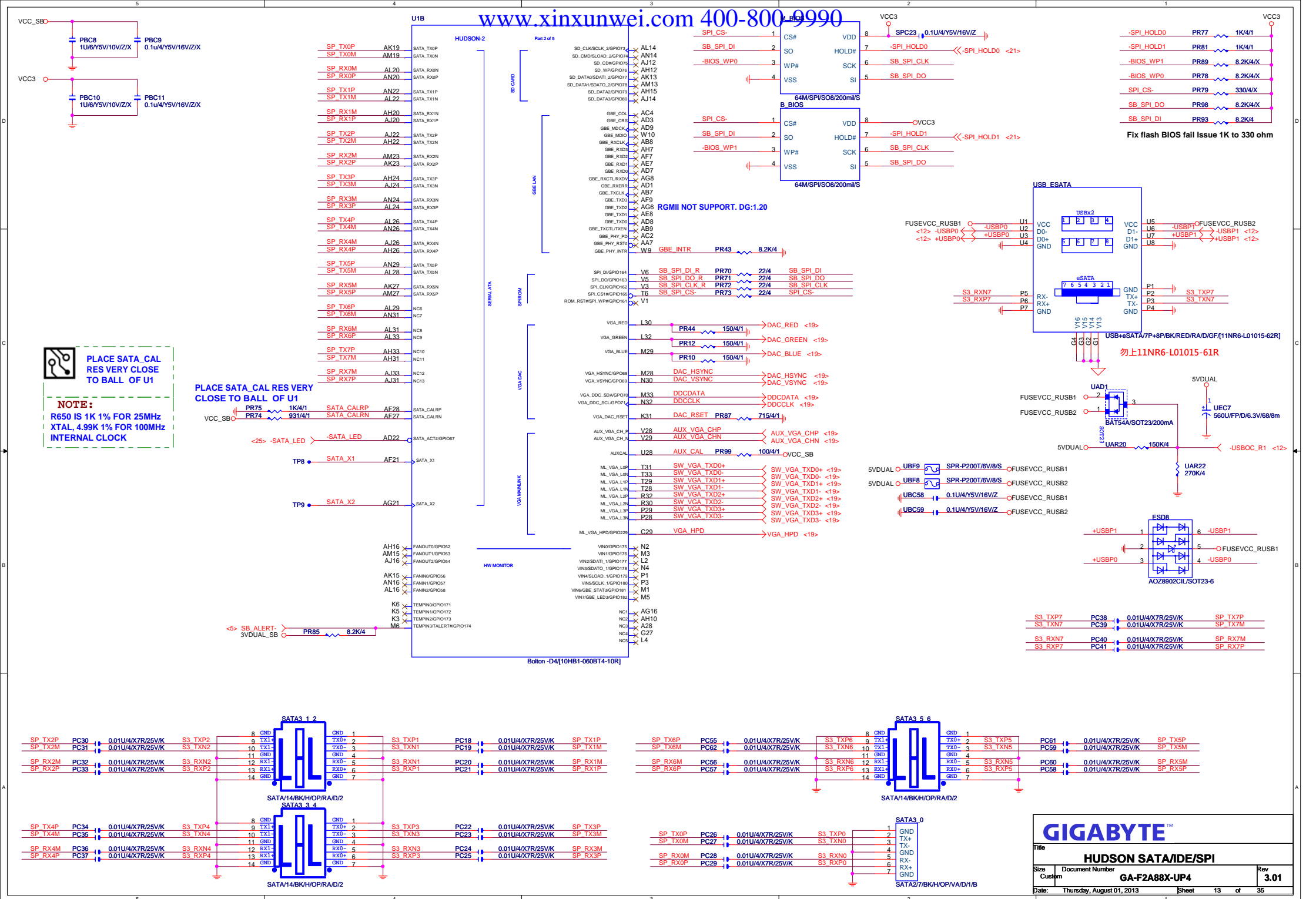
ROM TYPE:

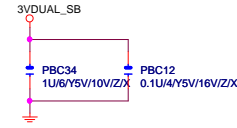
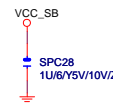
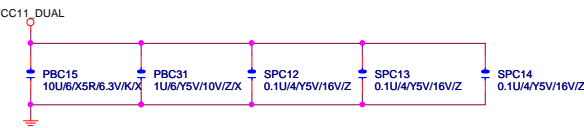
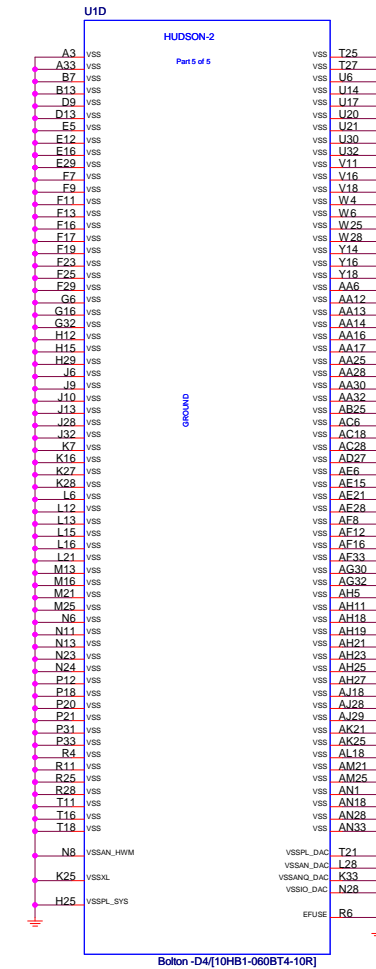
H = LPC RO

L = SPI ROM

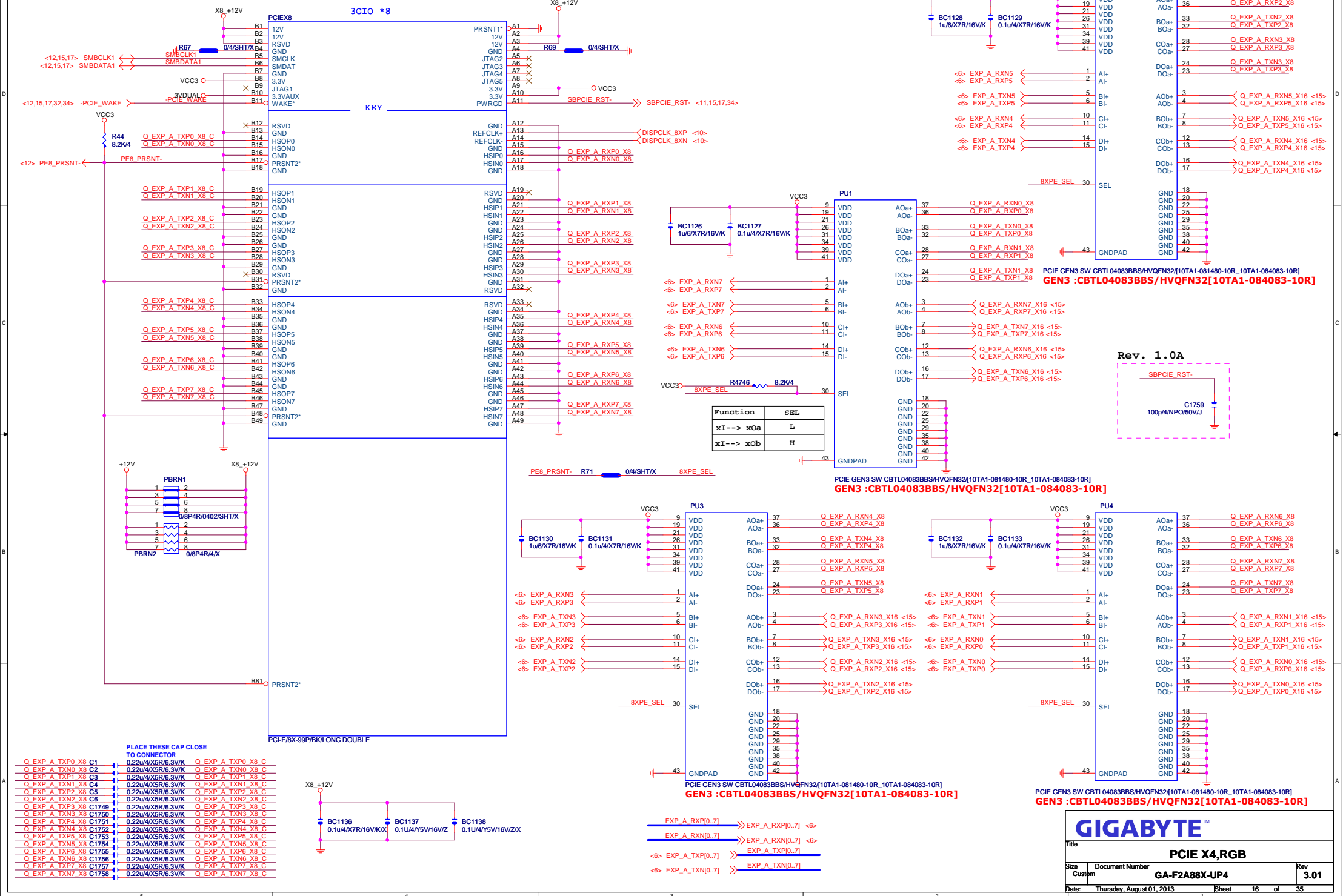
Bolton -D4/10HB1-060BT4-10R

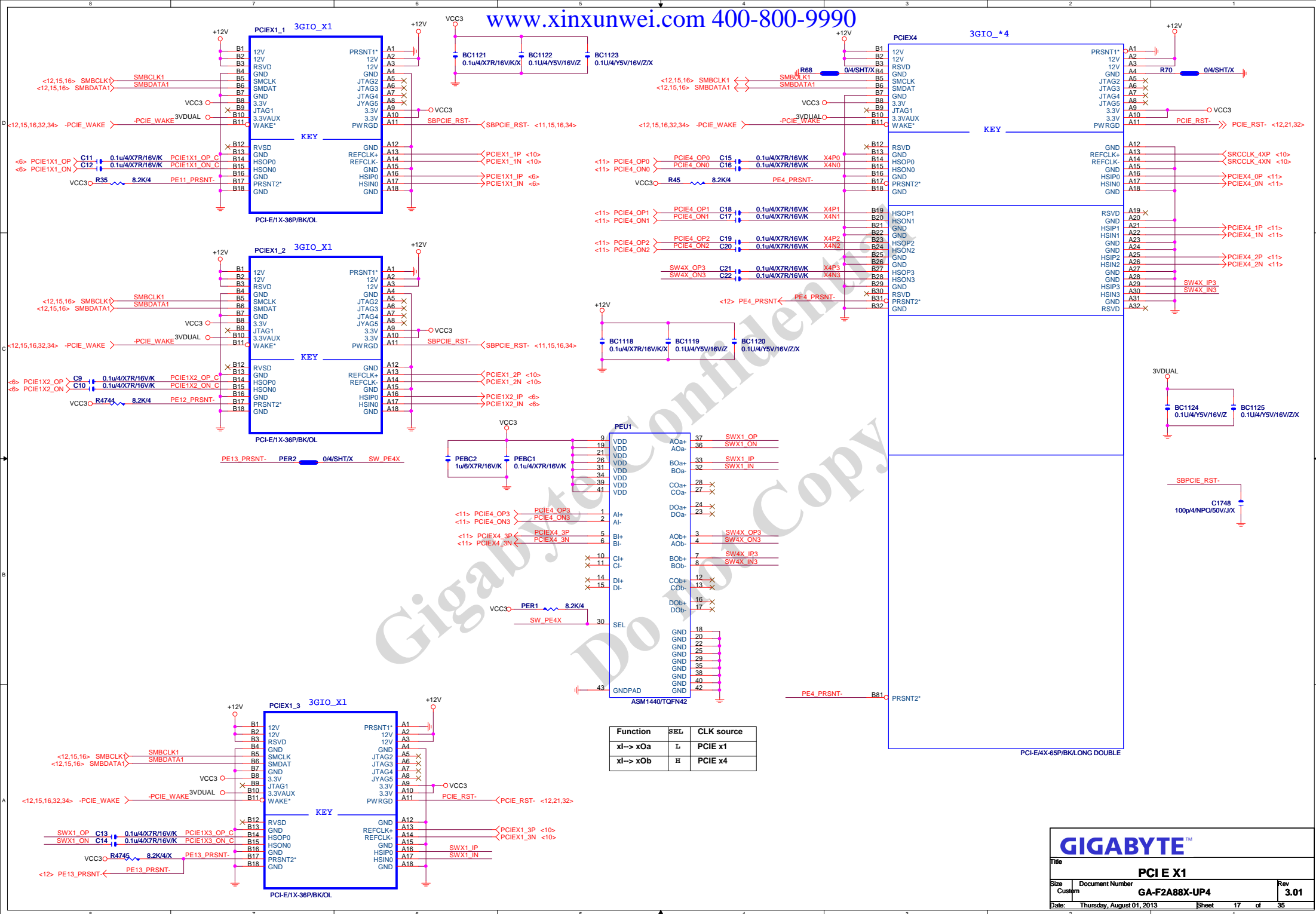
USB9	FRONT PANEL
USB8	FRONT PANEL
USB7	FRONT PANEL
USB6	FRONT PANEL
USB5	FRONT PANEL
USB4	FRONT PANEL
USB3	FRONT PANEL
USB2	FRONT PANEL
USB1	REAR PANEL
USB0	REAR PANEL











PCI SLOT 1,2

<11> AD[0..31] <-> AD[0..31]

PCI SLOT

PCI

B1

B2

B3

B4

B5

B6

B7

B8

B9

B10

B11

B12

B13

B14

B15

B16

B17

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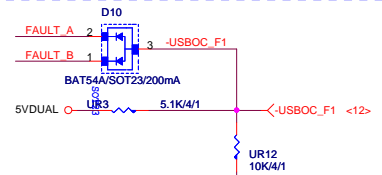
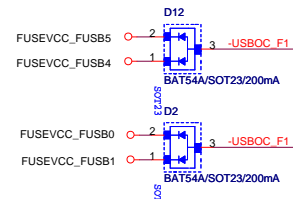
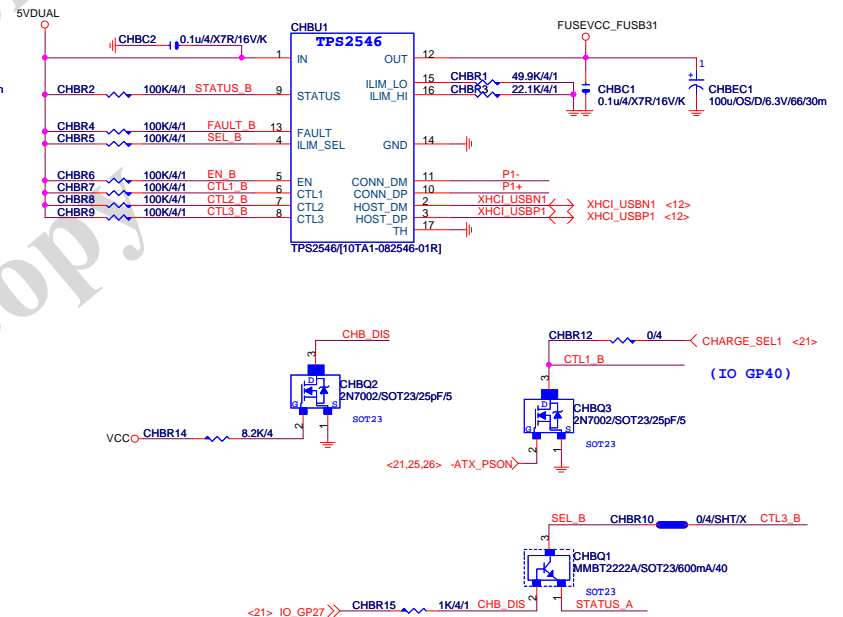
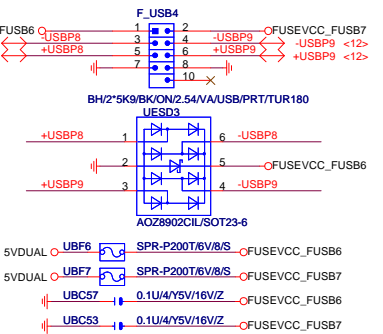
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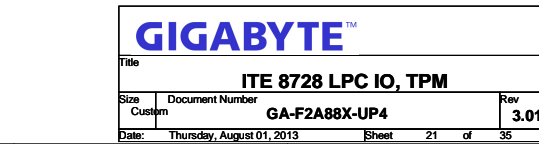
B342

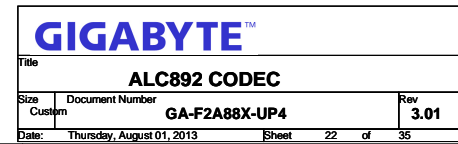
B343

B344

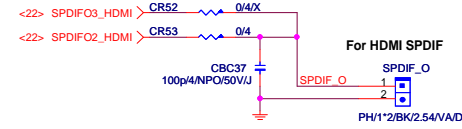
B345



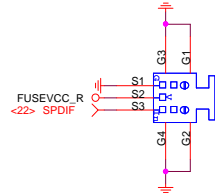




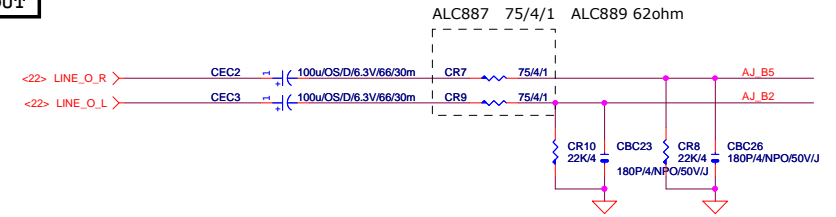
SPDIF



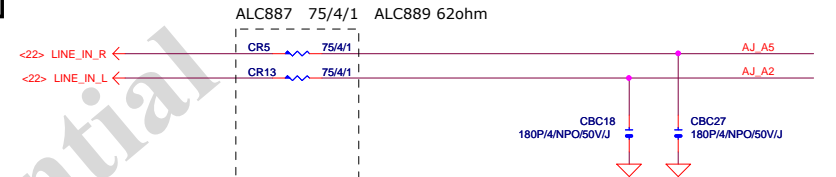
DP_HDMI_SPDIFC



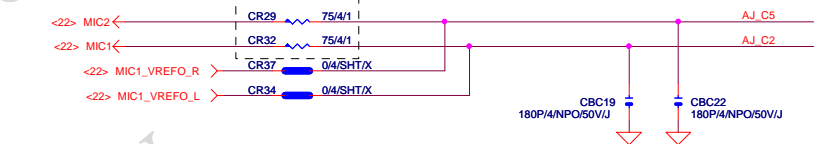
DP+HDMI+SPDIF/20P+19P+3P/BK/RA:DP_HDMI_SPDIF

LINE OUT
FRONT OUT

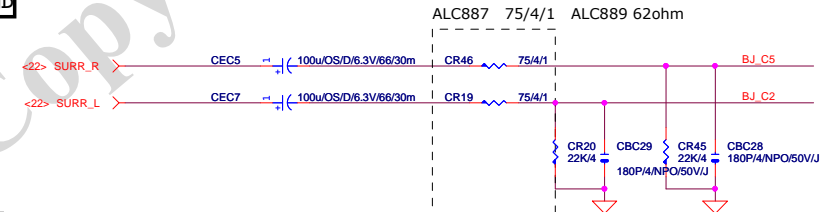
LINE-IN



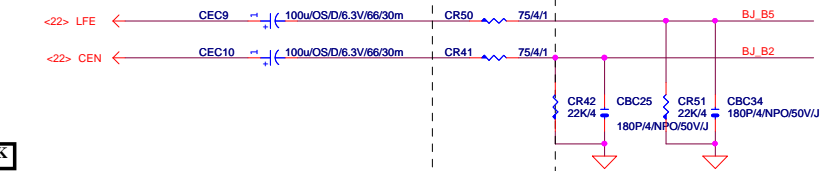
MIC



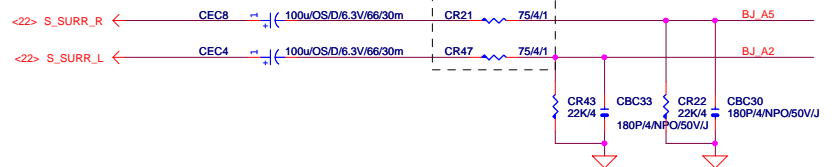
SURROUND



CEN/LFE



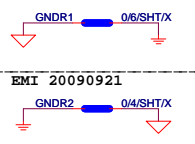
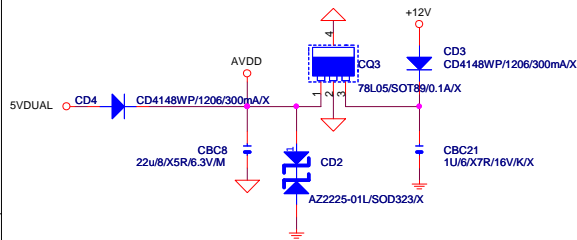
SURR BACK



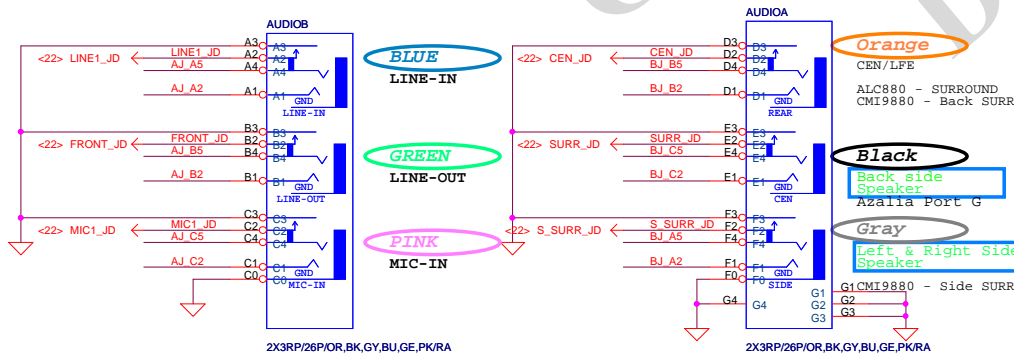
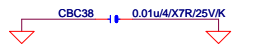
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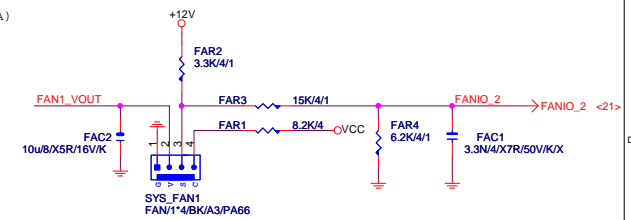
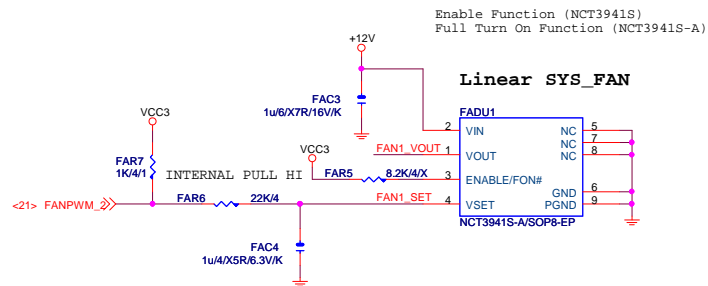
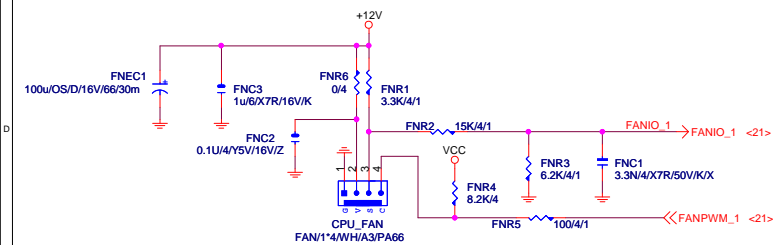
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AUDIO JACK		
Size	Document Number	Rev
Custom	GA-F2A88X-UP4	3.01
Date:	Thursday, August 01, 2013	Sheet 23 of 35

For ESD PROTECT DIODE

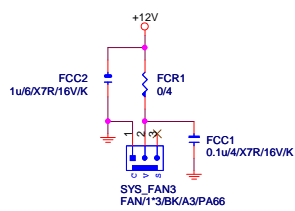


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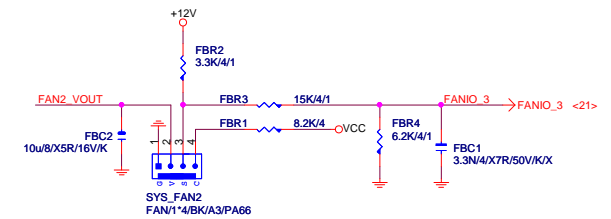
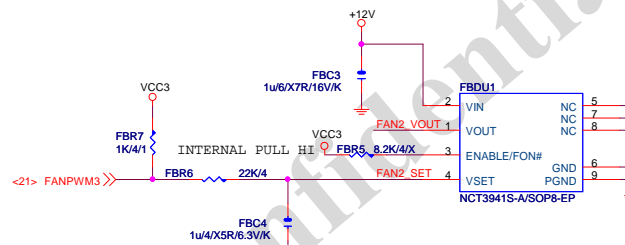
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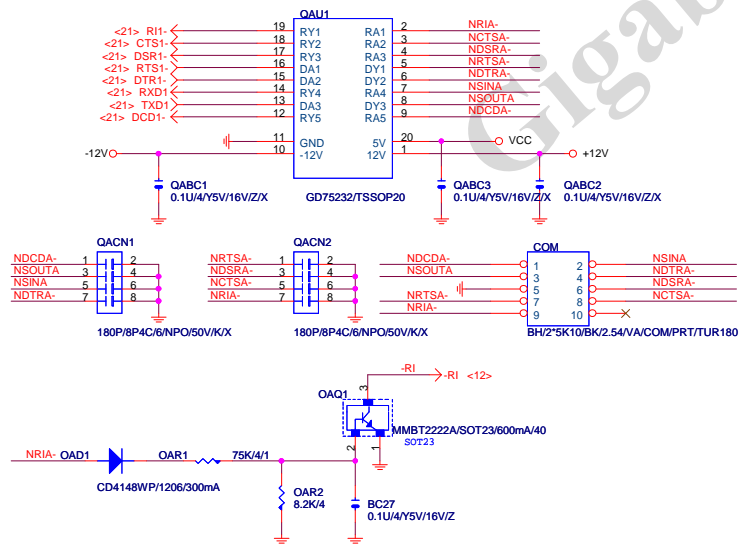
SYSTEM FAN3	PWR FAN
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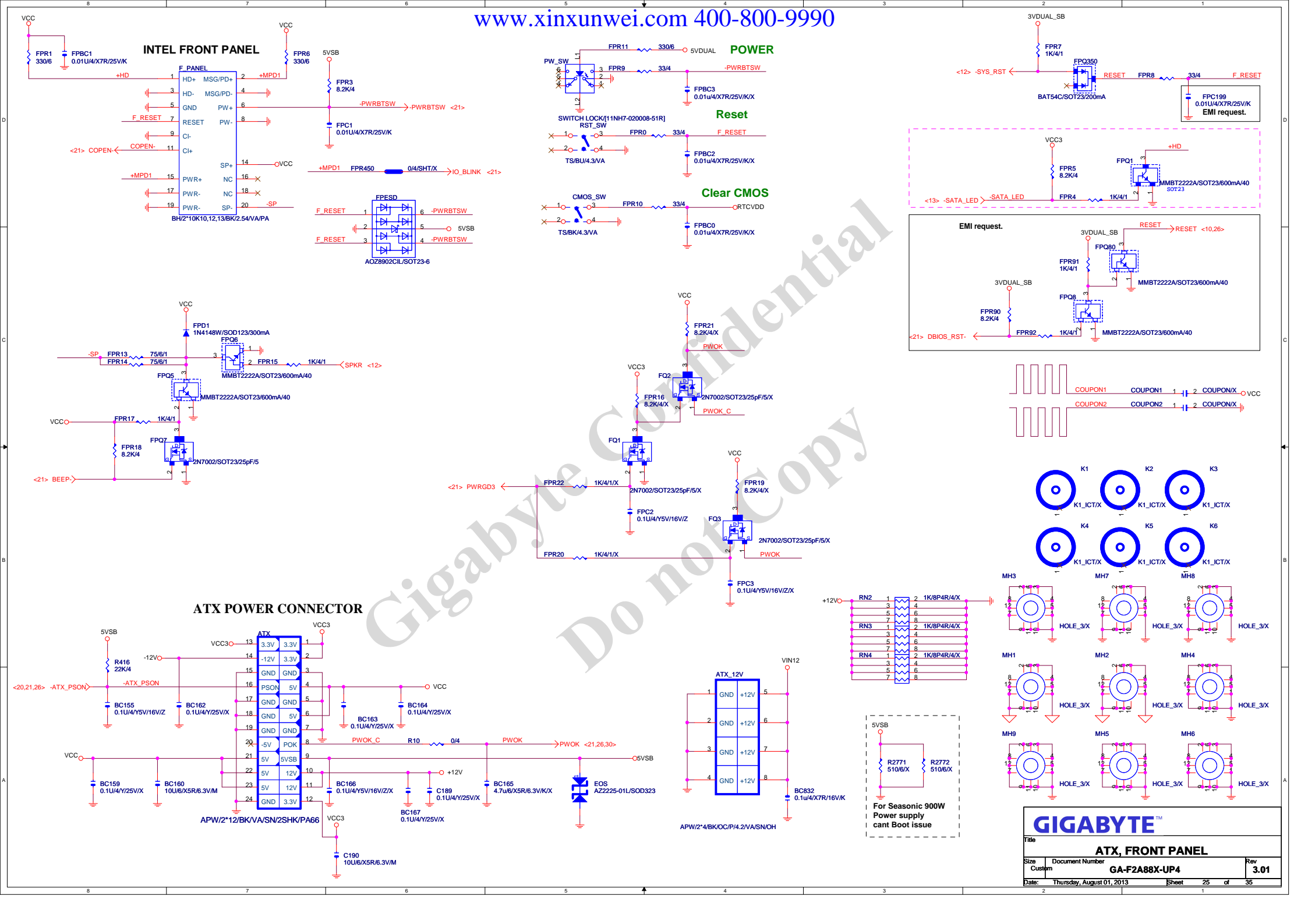
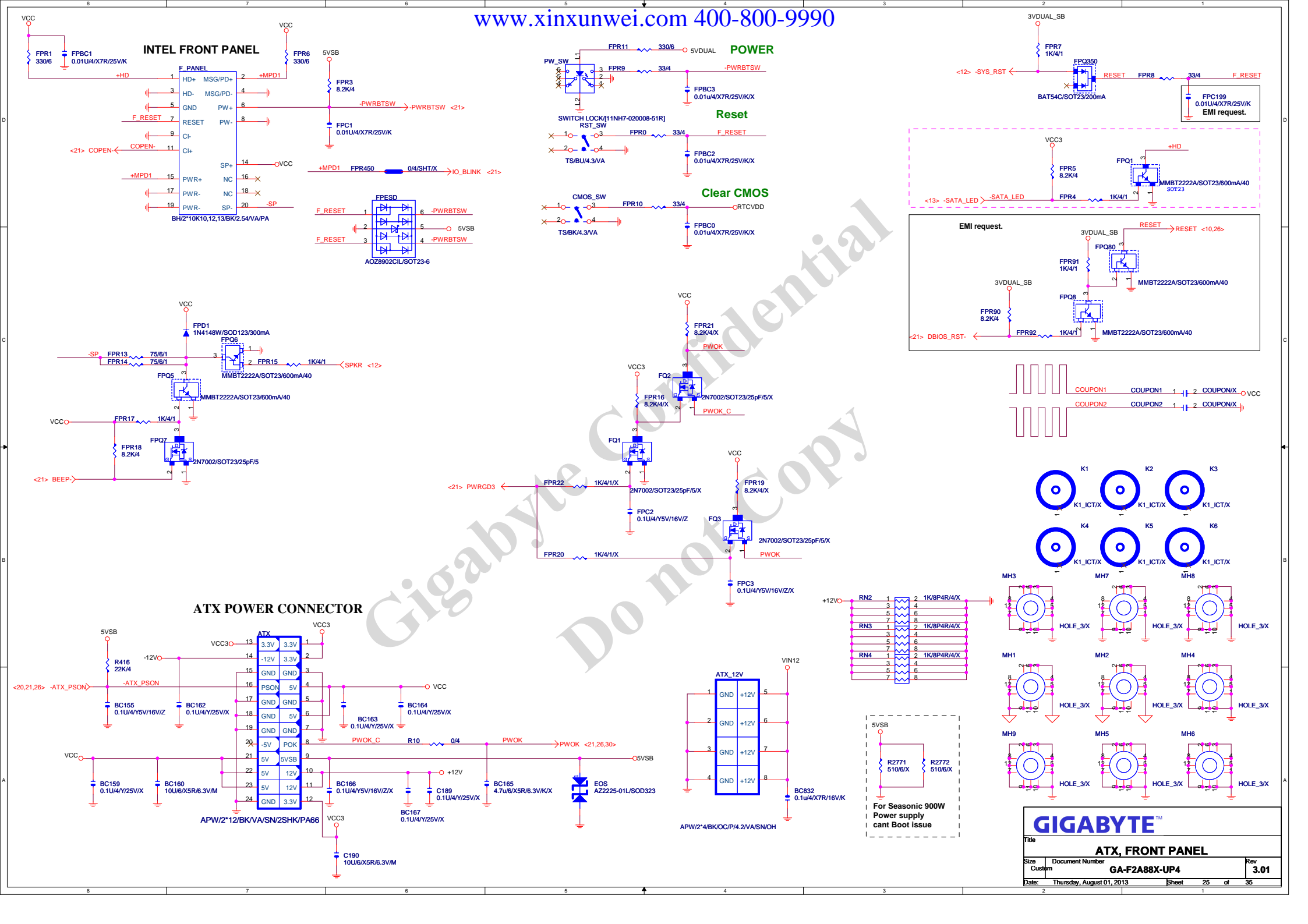
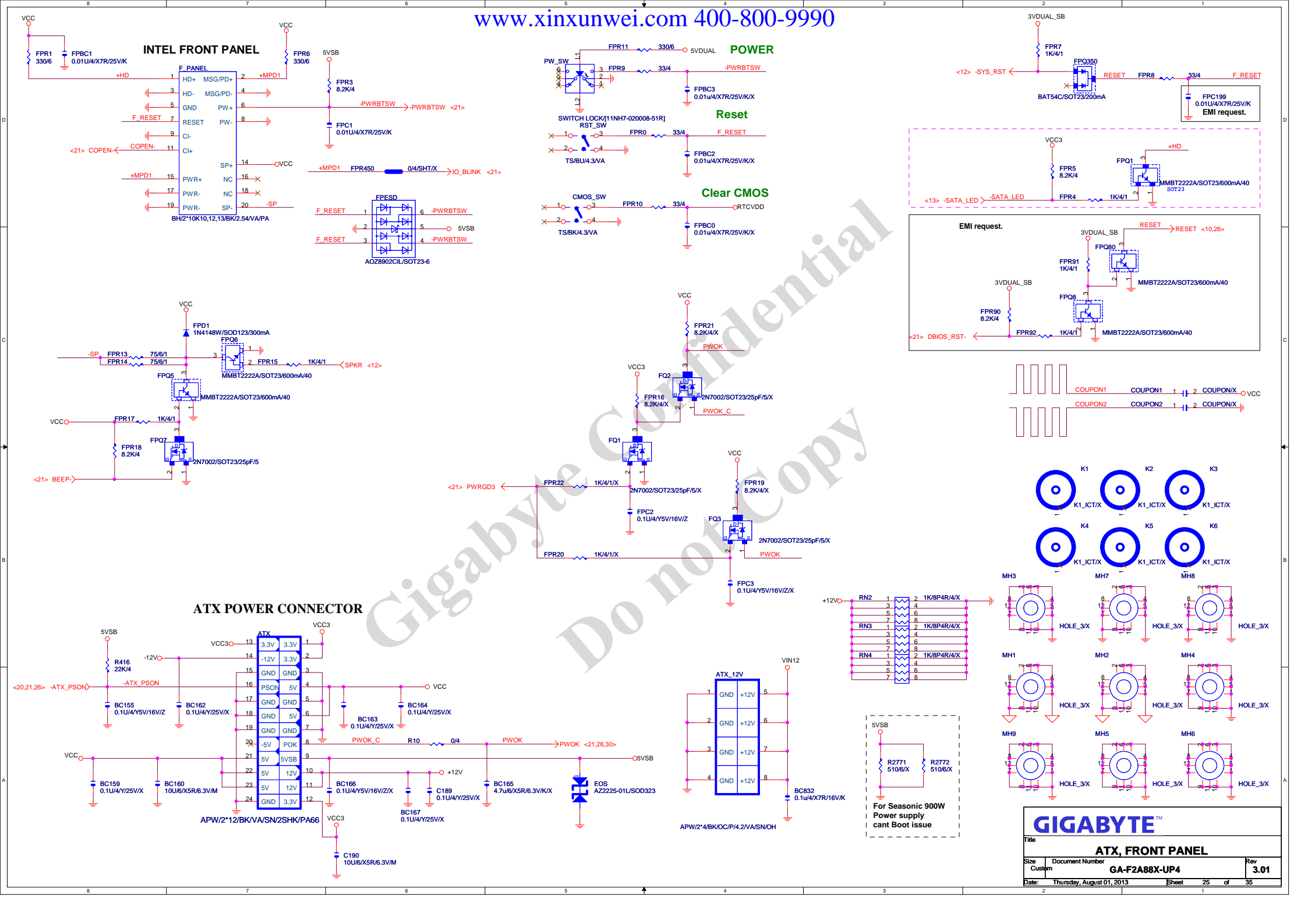


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SYSTEM FAN2 Voltage Mode
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COM PORT



[illegible]

INTEL FRONT PANEL

POWER

Reset

Clear CMOS

EMI request.

ATX POWER CONNECTOR

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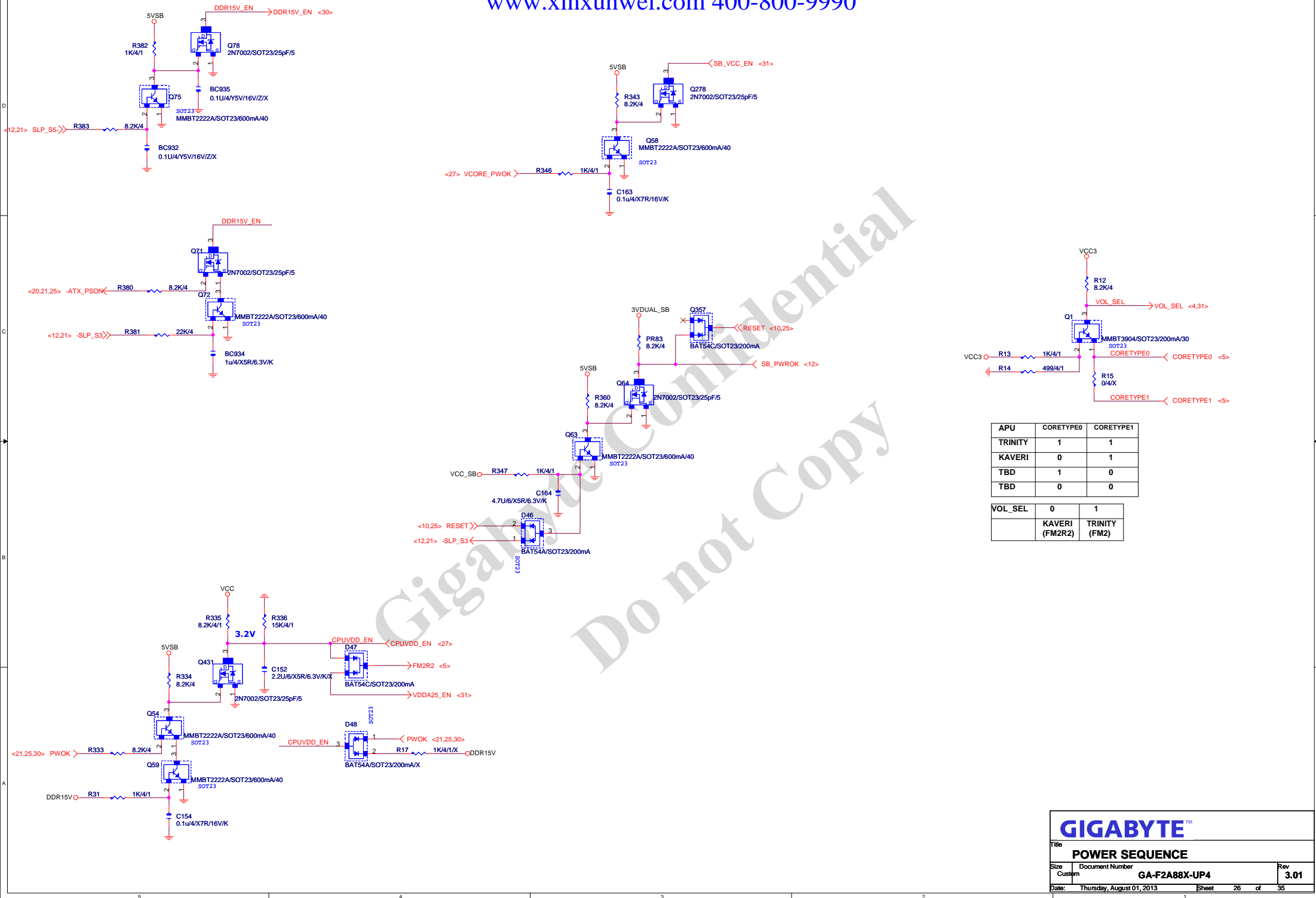
ATX, FRONT PANEL

GA-F2A88X-UP4

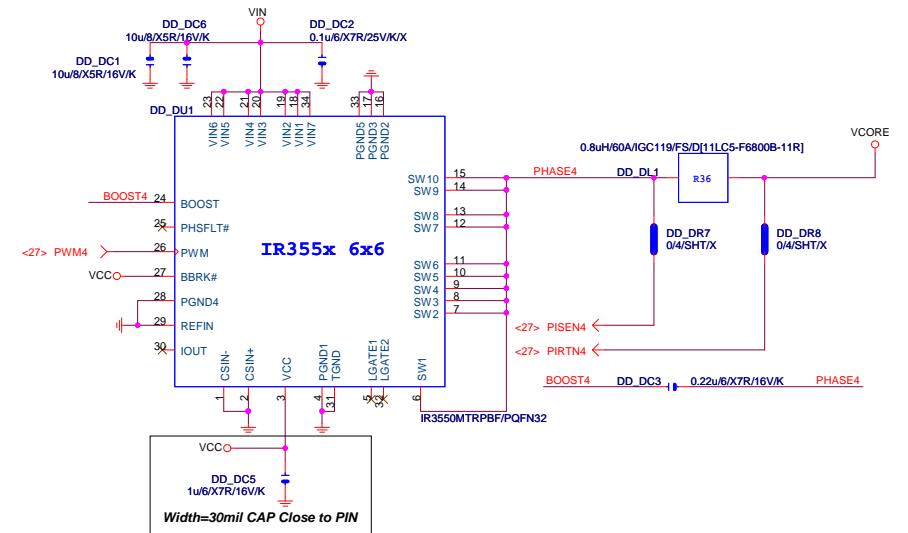
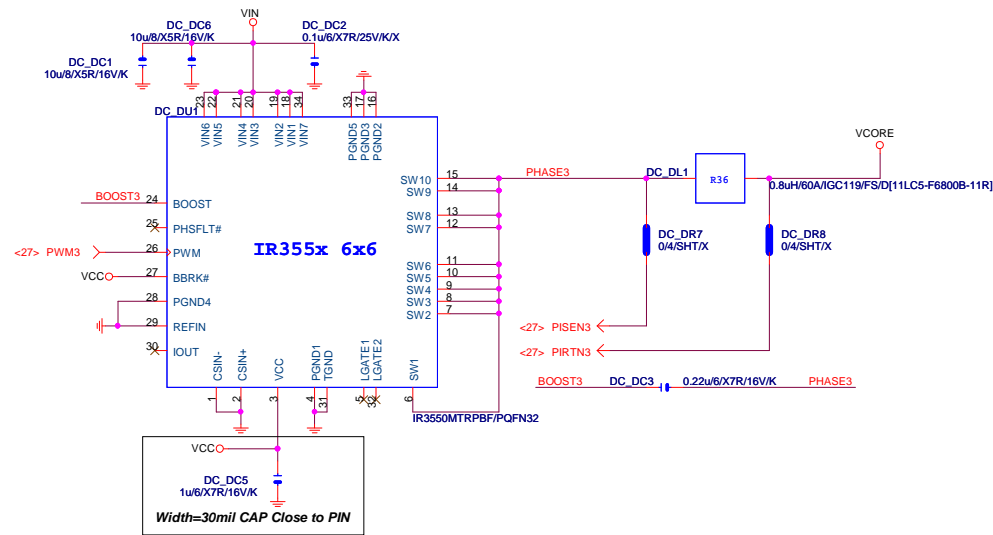
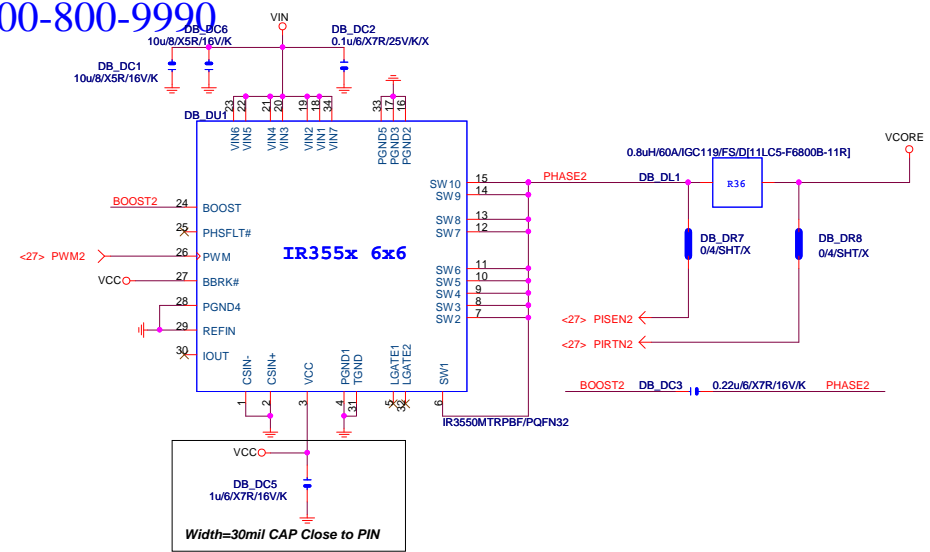
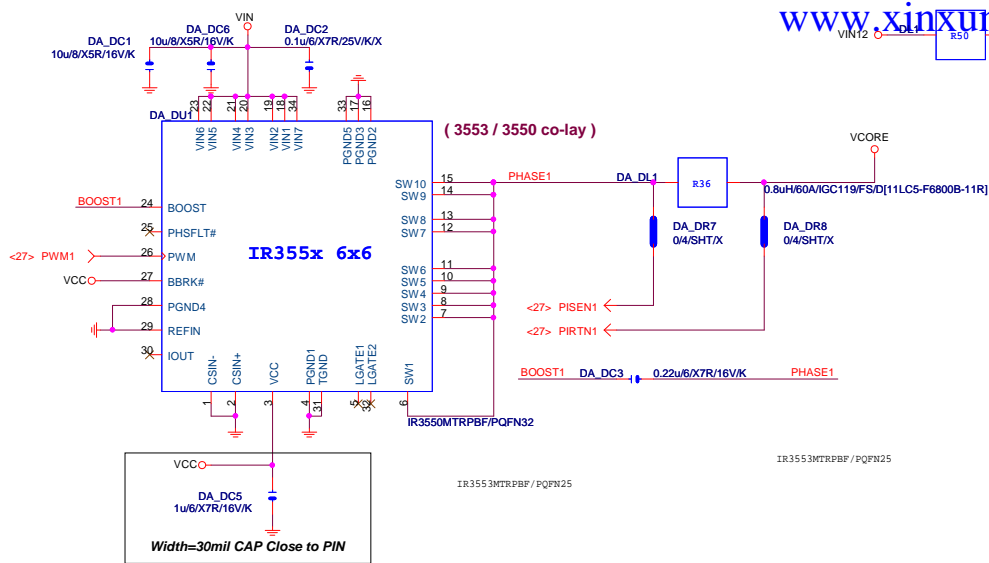
Rev 3.01

Date: Thursday, August 01, 2013 Sheet 25 of 35

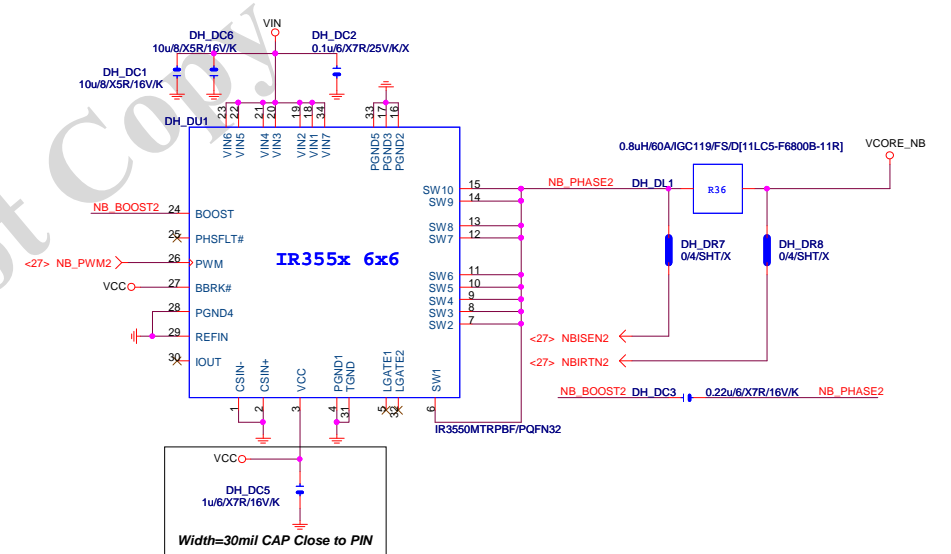
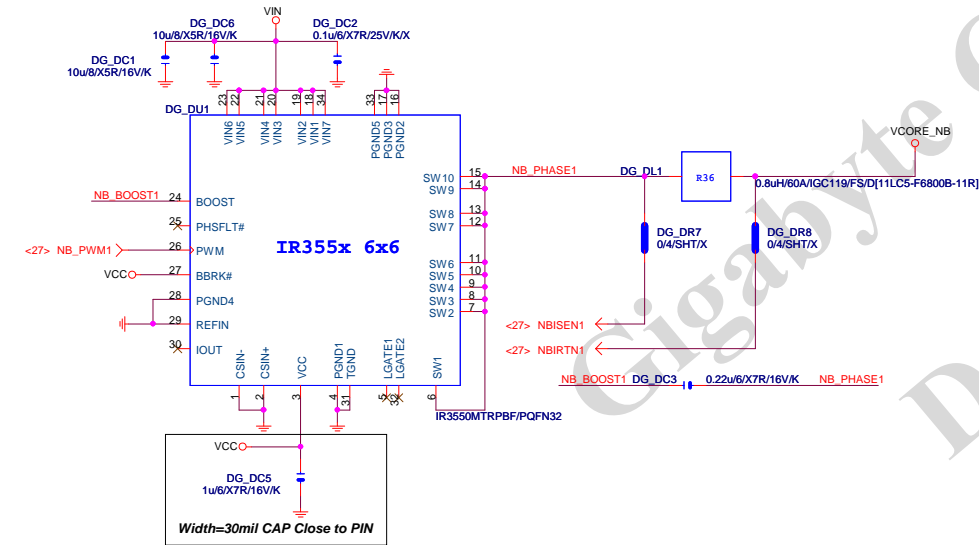
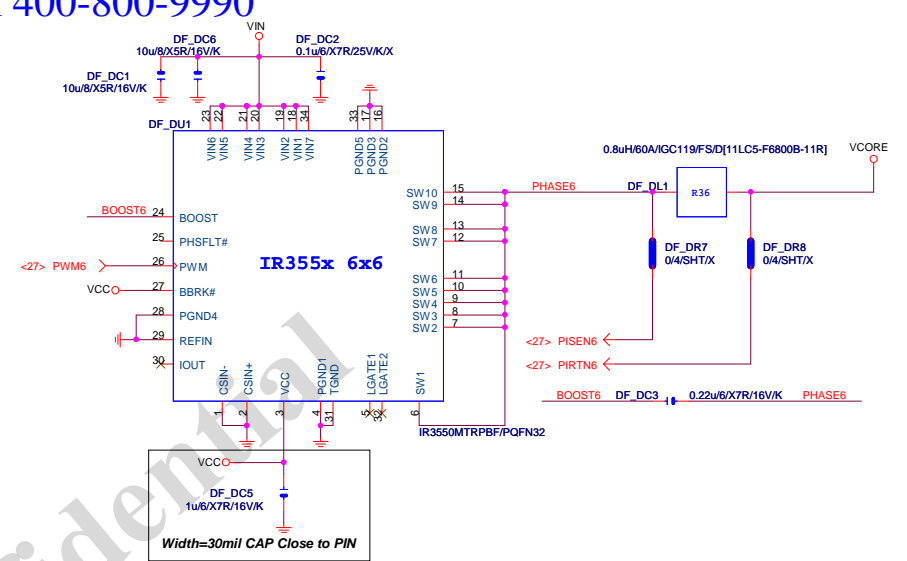
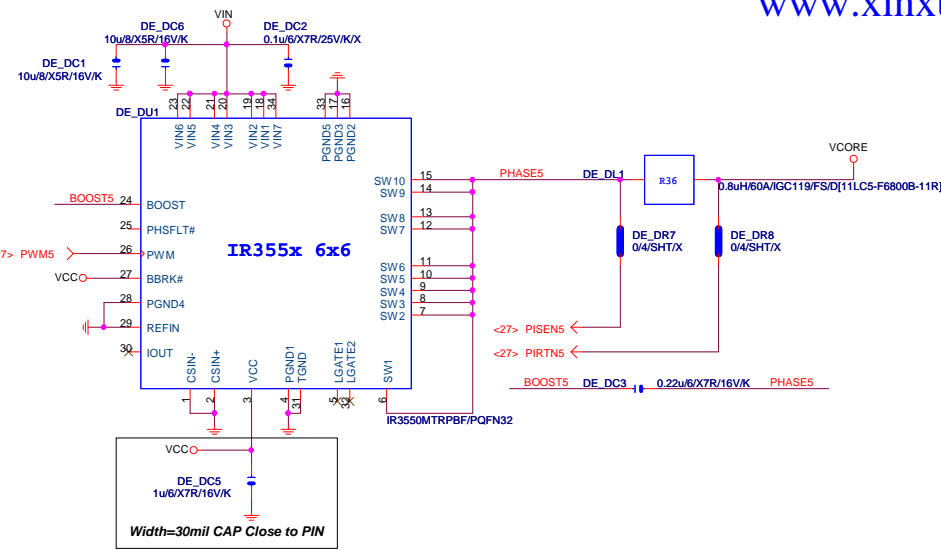
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GIGABYTE
POWER SEQUENCE

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 Size: Custom
 Document Number: **GA-F2A88X-UP4**
 Date: Thursday, August 01, 2013
 Rev: **3.01**
 Sheet: 26 of 35

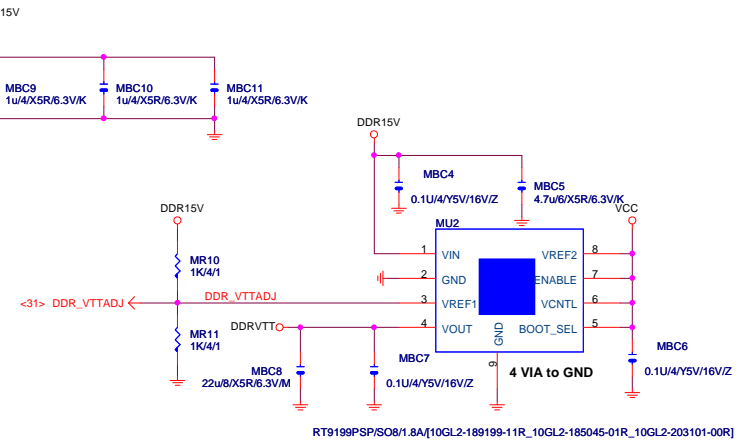
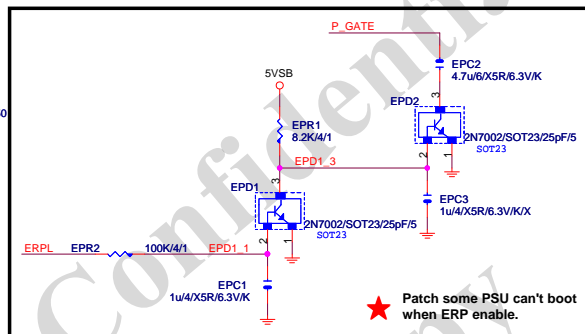
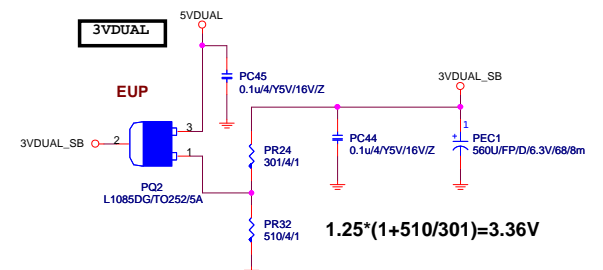
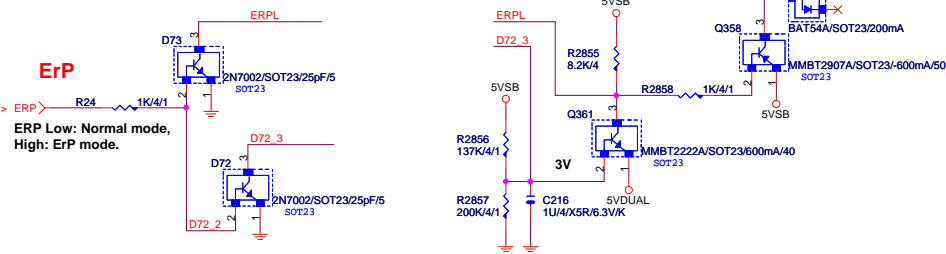
**GIGABYTE™**

Title		
VCORE MOSFET		
Size	Document Number	Rev
Custom	GA-F2A88X-UP4	3.01
Date: Thursday, August 01, 2013		
Sheet 28 of 35		



GIGABYTE™

Title			VIA VT6308P
Size	Document Number	Rev	
Custom	GA-F2A88X-UP4	3.01	
Date:	Thursday, August 01, 2013	Sheet	29 of 35

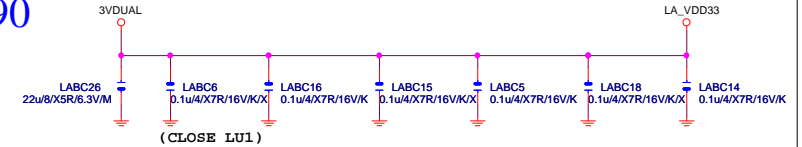
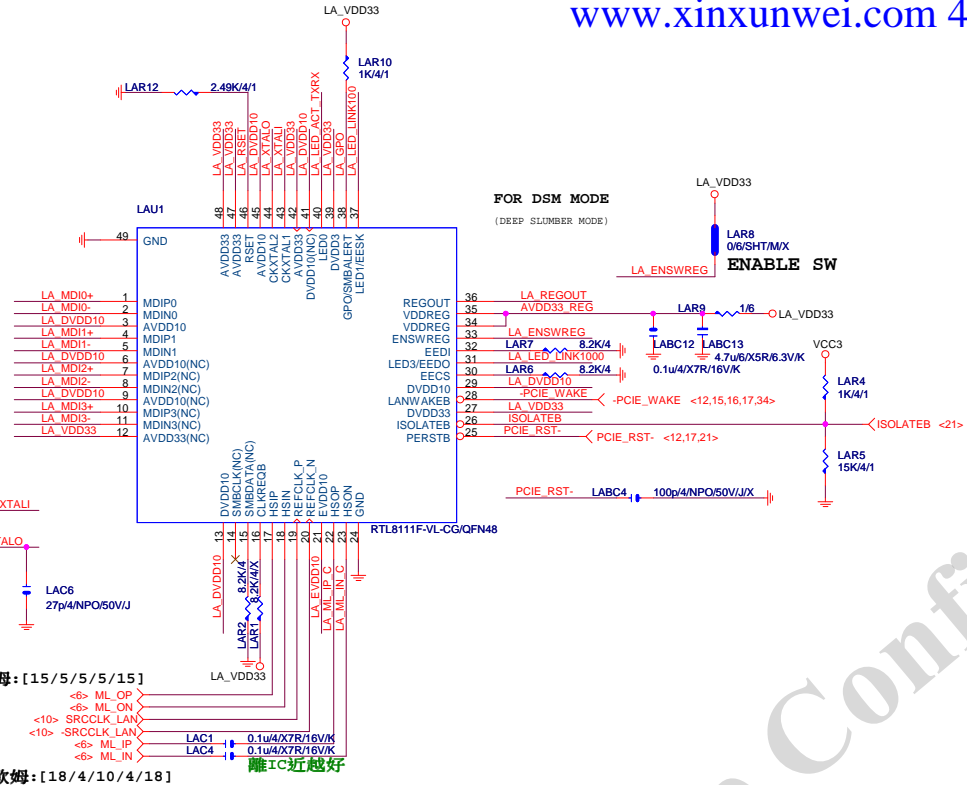


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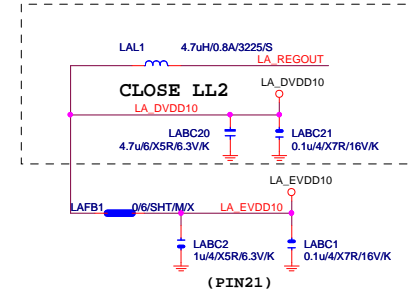
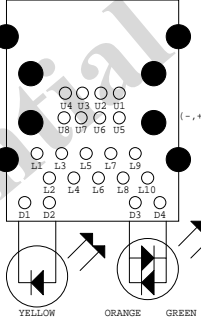
PCIE-1G LAN

Power domain chart

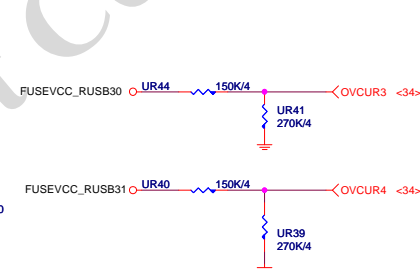
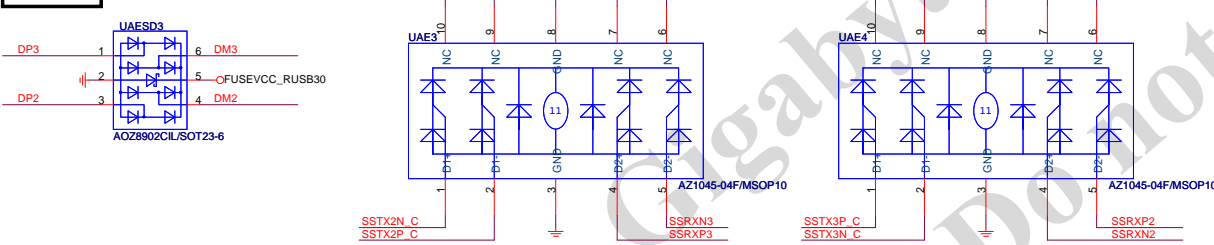
	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V



P35-152-19W9

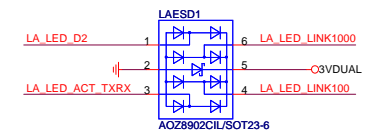
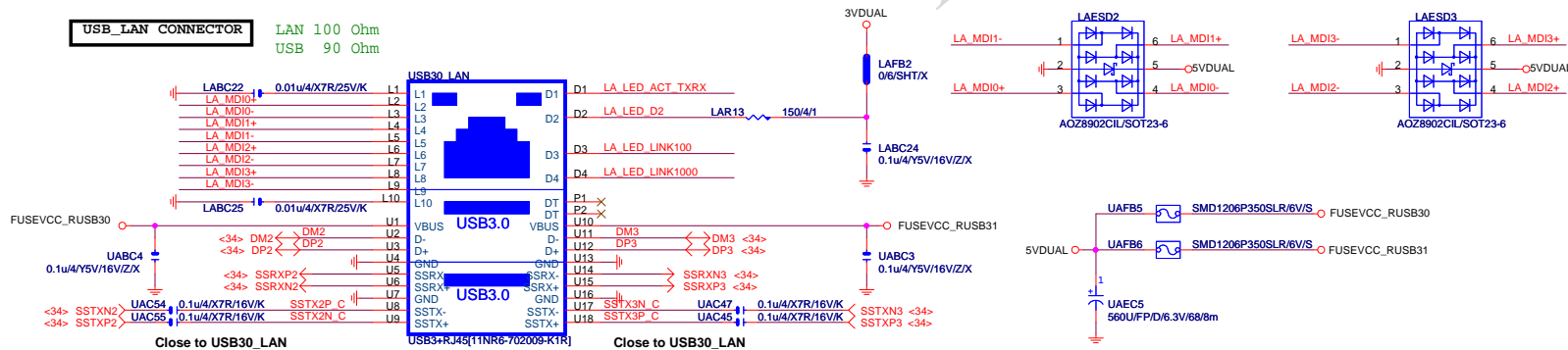


USB LAN



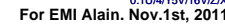
USB LAN CONNECTOR

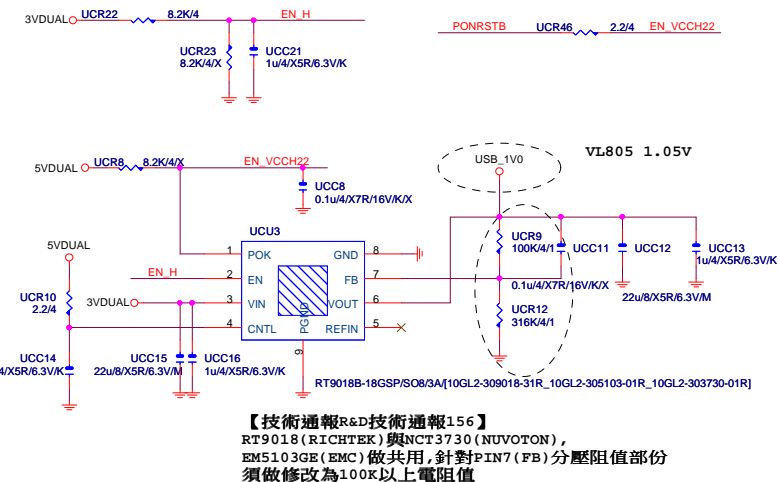
LAN 100 Ohm
USB 90 Ohm



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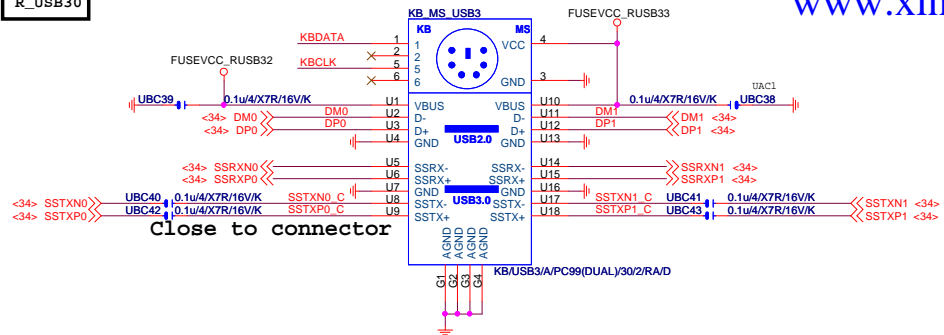
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Size	Document Number	Rev	
Custom	GA-F2A88X-UP4	3.01	
Date:	Thursday, August 01, 2013	Sheet	32 of 35



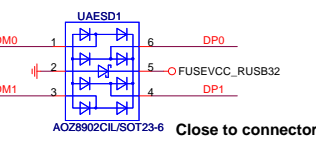
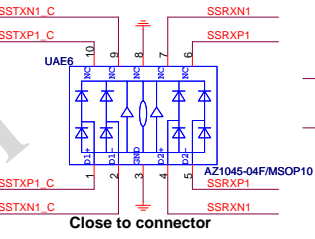
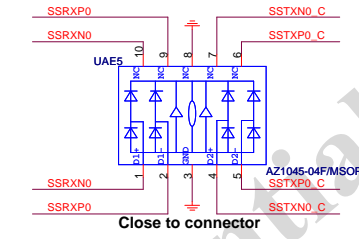
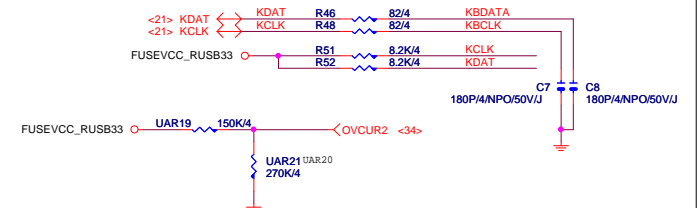
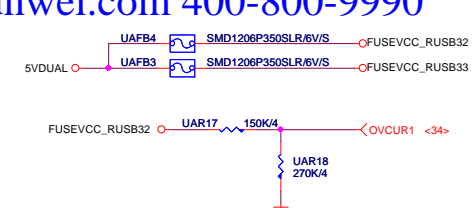


【技術通報R&D技術通報156】
RT9018(RICHTEK)與NCT3730(NUVOTON),
EM5103GE(EMC)做共用,針對PIN7(FB)分壓阻值部份
須做修改為100K以上電阻值

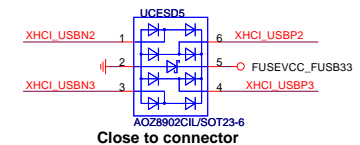
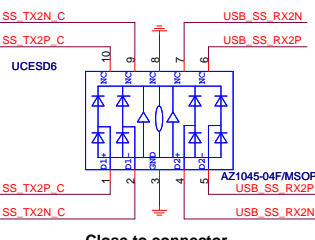
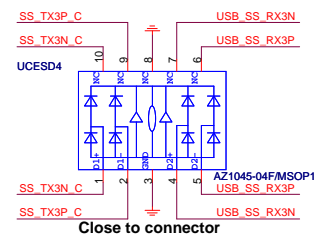
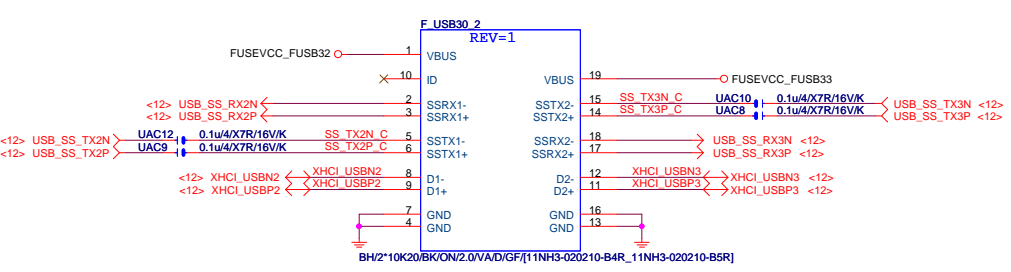
R_USB30



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F_USB30



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Title: USB3 VL805 R_USB & ESD Protect PS_KBMS

Size: Custom

Document Number: GA-F2A88X-UP4

Date: Thursday, August 01, 2013

Sheet: 35 of 35

Rev: 3.01